Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of modeling for use with an integrated circuit (IC) design, the method comprising the steps of:

partitioning an edge of a shape in the IC design into a plurality of intervals; and

assigning at least one dimension to each interval.

[c2] 2. The method of claim 1, wherein the partitioning step includes:

generating a core Voronoi diagram for the shape; and

partitioning the edge based on the core Voronoi diagram.

[c3] 3. The method of claim 2, wherein the core Voronoi diagram is generated based on the L∞ metric, and the assigning is based on a Euclidean metric.

[c4] 4. The method of claim 2, wherein the partitioning step further includes partitioning the edge based on a core element for each vertex of the core Voronoi diagram.

[c5] 5. The method of claim 4, wherein the core element is one of a largest possible core element and a smallest possible core element.

[c6] 6. The method of claim 5, wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and
wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

[c7] 7. The method of claim 1, wherein the at least one dimension includes a width for each interval and a spacing to a neighboring shape for each interval.

[c8] 8. The method of claim 1, wherein the dimension is a function of another dimension.

[c9] 9. The method of claim 1, further comprising the step of using the at least one dimension to evaluate a check rule.

[c10] 10. The method of claim 9, wherein the check rule involves at least one of: a single edge, a pair of neighboring edges, and edges within more than one layer of the IC design.

[c11] 11. The method of claim 1, wherein each concave vertex of the shape is an interval.

[c12] 12. An integrated circuit (IC) modeling system comprising:

means for partitioning an edge of a shape in the IC design into a plurality of intervals; and

means for assigning at least one dimension to each interval.

[c13] 13. The system of claim 12, wherein the partitioning means includes:

means for generating a core Voronoi diagram for the shape; and

means for partitioning the edge based on the core Voronoi diagram.

[c14] 14. The system of claim 13, wherein the partitioning means further includes means for partitioning the edge based on a core element for each vertex of the core Voronoi diagram.

[c15] 15. The system of claim 14, wherein the core element is one of a largest possible core element and a smallest possible core element.

[c16] 16. The system of claim 15, wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and

wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

[c17] 17. The system of claim 12, wherein the at least one dimension includes a width for each interval and a spacing to a neighboring shape for each interval.

[c18] 18. The system of claim 12, wherein the dimension is a function of another dimension.

[c19] 19. The system of claim 12, further comprising means for using the at least one dimension to evaluate a check rule.

[c20] 20. The system of claim 19, wherein the check rule involves at least one of: a single edge, a pair of neighboring edges, and edges within more than one layer of the IC design.

[c21] 21. A computer program product comprising a computer useable medium having computer readable program code embodied therein for modeling an integrated circuit, the program product comprising:

program code configured to partition an edge of a shape in the IC design into a plurality of intervals; and

program code configured to assign at least one dimension to each interval.

[c22] 22. The program product of claim 21, wherein the parti-

tioning code includes:

program code configured to generate a core Voronoi diagram for the shape; and

program code configured to partition the edge based on the core Voronoi diagram.

[c23] 23. The program product of claim 22, wherein the partitioning code further includes program code configured to partition the edge based on a core element for each vertex of the core Voronoi diagram.

[c24] 24. The program product of claim 23, wherein the core element is one of a largest possible core element and a smallest possible core element.

[c25] 25. The program product of claim 24, wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

[c26] 26. The program product of claim 22, wherein the at least one dimension includes a width for each interval and a spacing to a neighboring shape for each interval.

[c27] 27. The program product of claim 22, wherein the at least one dimension is a function of another dimension.

[c28] 28. The program product of claim 22, further comprising the program code configured to use the dimensions to evaluate a check rule.

[c29] 29. The program product of claim 28, wherein the check rule involves at least one of: a single edge, a pair of neighboring edges, and edges within more than one layer of the IC design.

[c30] 30. An integrated circuit (IC) check rule evaluation system comprising:

means for partitioning an edge of a shape in the IC design into a plurality of intervals, the partitioning means including:

means for generating a core Voronoi diagram for the shape using a first metric, and

means for partitioning the edge based on the core Voronoi diagram;

means for assigning at least one dimension to each interval using a second metric; and

means for using the at least one dimension to evaluate a check rule.

[c31] 31. The IC check rule evaluation system of claim 30, wherein the check rule is a width dependent spacing rule.